## CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being transmitted via the USPTO-EFS-Web to Examiner Dilton J. Cody on May 22, 2006.

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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In Re Application of: Date: May 22, 2006

Andreas DOERING et al. Confirmation No: 8071

Serial No: 10/696,865 Group Art Unit; 2183

Filed: October 30, 2003 Examiner: Cody, Dillon J.

For: METHOD AND APPARATUS FOR USING FPGA TECHNOLOGY WITH A MICROPROCESSOR FOR RECONFIGURABLE INSTRUCTION LEVEL

HARDWARE ACCELERATION

Mail Stop Amendment Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

## AMENDMENT IN REPLY TO ACTION OF FEBRUARY 22, 2006

In response to the Office Action dated February 22, 2006, please amend the application identified above as follows:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 11 of this paper.

Remarks begin on page 20 of this paper.